

		Subclass	ISSUE CLASSIFICATION
	Class		

**PATENT NUMBER**

**U.S. UTILITY Patent Application**

O.I.P.E.	PATENT DATE
H.T. <i>[Signature]</i>	
SCANNED <i>[Signature]</i>	Q.A. <i>[Signature]</i>

APPLICATION NO. 09/843228	CONT/PRIOR	CLASS 709	SUBCLASS 213	ART UNIT 215E	EXAMINER BROWN S.
------------------------------	------------	--------------	-----------------	------------------	----------------------

APPLICANTS

Simon Steely  
Madhumitra Sharma  
Stephen Van Doren

## Low latency inter-reference ordering in a multiple processor system employing a multiple-level inter-node switch

E

PTO-2040  
12/99

## **ISSUING CLASSIFICATION**

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.				<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____				<b>ISSUE FEE</b>	
	(Assistant Examiner)	(Date)		Amount Due	Date Paid
<input type="checkbox"/> The terminal ____ months of this patent have been disclaimed.				<b>ISSUE BATCH NUMBER</b>	
	(Primary Examiner)	(Date)		(Legal Instruments Examiner)	

**WARNING:**

The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436A  
(Rev. 6/99)

FILED WITH:  DISK (CRF)  FICHE  CD-ROM  
(Attached in pocket on right inside flap)

(FACE)